

What is claimed is:

1. A method, comprising:
providing at least one buffer in an interface between a
chipset and memory modules, said at least one buffer allowing the
interface to be split into first and second sub-interfaces, where
the first sub-interface is between the chipset and the at least
one buffer, and the second sub-interface is between the at least
one buffer and the memory modules; and
configuring said at least one buffer to properly latch the
data being transferred between the chipset and the memory
modules, such that the first and second sub-interfaces operate
independently but in synchronization with each other.

2. The method of claim 1, wherein said providing said at
least one buffer isolates the first and second sub-interfaces in
such a manner that the first sub-interface is operated at
different voltage level than the second sub-interface.

3. The method of claim 2, wherein an operating voltage
level of said first sub-interface is less than 1.0 volt.

4. The method of claim 2, wherein an operating voltage
level of said second sub-interface is between 1.2 and 1.8 volts.

1 5. The method of claim 1, wherein said providing said at
2 least one buffer isolates the first and second sub-interfaces in
3 such a manner that the first sub-interface is operated at higher
4 frequency than the second sub-interface.

1 6. The method of claim 5, wherein said first sub-interface
2 is operated at twice the frequency of the second sub-interface.

1 7. The method of claim 6, wherein a number of data lines
2 in said first sub-interface is half that of a number of data
3 lines in said second sub-interface.

1 8. The method of claim 1, wherein said at least one buffer
2 are provided on a same memory board as the memory modules
3 corresponding to said at least one buffer.

1 9. The method of claim 1, wherein said chipset is provided
2 on a motherboard.

1 10. The method of claim 1, wherein said interface between
2 the chipset and the memory modules is a multidrop bus.

1 11. The method of claim 1, wherein each of said memory
2 modules includes dynamic random access memory (DRAM).

1 12. The method of claim 1, wherein each of said memory
2 modules includes double data rate (DDR) DRAM.

1 13. The method of claim 1, wherein each of said memory
2 modules includes quad data rate (QDR) DRAM.

1 14. A method, comprising:
2 providing at least one buffer in an interface between a
3 chipset and memory modules, said at least one buffer allowing the
4 interface to be split into first and second sub-interfaces, where
5 the first sub-interface is between the chipset and the at least
6 one buffer, and the second sub-interface is between the at least
7 one buffer and the memory modules, said at least one buffer
8 isolates the first and second sub-interfaces in such a manner
9 that the first sub-interface is operated at different voltage
10 level than the second sub-interface, and the first sub-interface
11 is operated at higher frequency than the second sub-interface;
12 and

13 configuring said at least one buffer to properly latch the
14 data being transferred between the chipset and the memory
15 modules, such that the first and second sub-interfaces operate
16 independently but in synchronization with each other.

1 15. The method of claim 14, wherein said providing said at
2 least one buffer isolates the first and second sub-interfaces in
3 such a manner that the first sub-interface is operated at
4 different voltage level than the second sub-interface.

1 16. The method of claim 14, wherein said providing said at
2 least one buffer isolates the first and second sub-interfaces in
3 such a manner that the first sub-interface is operated at higher
4 frequency than the second sub-interface.

1 17. A method, comprising:

2 isolating a memory interface between a chipset and memory
3 modules, where said isolating divides the memory interface into
4 first and second sub-interfaces; and

5 configuring said first and second sub-interfaces to properly
6 transfer data between the chipset and the memory modules, such
7 that the first and second sub-interfaces operate independently
8 but in synchronization with each other,

9 wherein said first and second sub-interfaces are configured
10 in such a manner that the first sub-interface is operated at
11 different voltage level and at higher frequency than the second
12 sub-interface.

1 18. The method of claim 17, wherein an operating voltage
2 level of said first sub-interface is less than 1.0 volt, and an
3 operating voltage level of said second sub-interface is between
4 1.2 and 1.8 volts.

1 19. The method of claim 17, wherein said first sub-
2 interface is operated at twice the frequency of the second sub-
3 interface, and a number of data lines in said first sub-interface
4 is half that of a number of data lines in said second sub-
5 interface.

1 20. A system, comprising:
2 a memory interface between a chipset and at least one memory
3 module; and

4 at least one buffer disposed in said memory interface to
5 divide said memory interface into first and second sub-
6 interfaces,

7 where said first and second sub-interfaces are configured in
8 such a manner that the first sub-interface is operated at
9 different voltage level and at higher frequency than the second
10 sub-interface.

1 21. The system of claim 20, wherein an operating voltage
2 level of said first sub-interface is less than 1.0 volt, and an
3 operating voltage level of said second sub-interface is between
4 1.2 and 1.8 volts.

1 22. The system of claim 20, wherein said first sub-
2 interface is operated at twice the frequency of the second sub-
3 interface.

1 23. The system of claim 22, wherein a number of data lines
2 in said first sub-interface is half that of a number of data
3 lines in said second sub-interface.

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